RADIATION RESISTANT BIPOLAR MEMORY

This application is a continuing application of application Ser. No. 042,698, filed Apr. 27, 1987, which is a continuation-in-part application of application Ser. No. 792,286, filed Oct. 28, 1985.

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to a semiconductor memory and, more particularly, to a bipolar memory having improved immunity to soft error attributable to the noise created by radiation such as alpha rays.

Further, the present invention relates to a high-speed diode construction resistant to noise from the substrate, employed as a load for the above-mentioned bipolar memory.

Still further, the present invention relates to a high-performance vertical transistor construction resistant to noise from the substrate, employed as a load for the above-mentioned bipolar memory.

2. Description of the Prior Art:

It is a well known fact that the incidence of alpha particles, though of a very small amount, radiated from the material forming the package (a container accommodating a semiconductor chip) into a semiconductor substrate produces electron-hole pairs, which can easily destroy the information stored in the semiconductor memory. Such destruction of information was found first in MOS memories. Thereafter, soft error has been found also in bipolar memories; and contriving measures to obviate soft error has been a significant problem in designing semiconductor memories.

Prior to the description of the present invention, the process of soft error in the bipolar memory attributable to alpha rays will be described.

FIGS. **1A** to **1I** are circuit diagrams of widespread conventional typical bipolar memory cells. The cells of FIGS. **1A** to **1E** have constructions securing high-speed operation at a low power consumption rate. In the non-selected state, a stand-by current is supplied to a load resistor having a high resistance to obtain a desired voltage swing, while in the selected state, the load is changed to a load having a low impedance in order to supply a large read (or write) current. FIGS. **1F** to **1I** show-cross-coupled pnpn cells particularly suitable for constructing a compact device. These cells are compact and suitable for constructing a large-capacity device, however, when an additional capacitance is given thereto to reinforce the alpha ray resistance, the memory cell area is increased to disadvantage.

FIG. **2** is a typical plan view of the memory cell of FIG. **1A**. In FIG. **2**, there are shown the terminals **3C**, **3B** and **3E** for the collector, the base and the emitter, respectively. FIG. **3** is a sectional view taken along line aa' of FIG. **2**. In FIG. **3**, n^- layer (epitaxial layer) **36** and n^+ buried layer (n^+ BL) **30** are a collector region. The diode of FIG. **1A** is formed between a p^+ layer **31** and the n^+ BL **30**. The resistance **12** (FIG. **1A**) is formed by a p layer **32** and the transistors (FIG. **1A**) are formed by emitter n^+ layers **33** and **34** and by a base p^+ layer **35** and the n^- layer **36**. Indicated at **301** is a thick insulating film for separating the devices.

When radiation, such as alpha rays, including the radiation radiated from the components of the IC, such as the package, and cosmic rays falls on the memory cell having such a sectional construction, a large amount of electron-hole pairs are produced within the semiconductor, as illustrated in FIG. **3**. As illustrated in FIG. **3**, more electron-hole pairs are produced within a silicon substrate **37** supporting the component devices (transistors, resistors, diodes and the like) of the memory cell than within those component devices. (Typically, the thicknesses of the n^- Ep layer **36** and the n^+ BL layer **30** are 1 to 2 μm, whereas the range of alpha particles is as large as 50 to 70 μm.) The electrons of the electron-hole pairs produced within the silicon substrate diffuse and approach the n^+ BL **30**. Upon the arrival at the depletion layer between the n^+ BL **30** and the silicon substrate **37** (p-substrate), the electrons are accelerated by the electric field of the depletion layer and reach the n^+ BL layer **30** (the collector of the transistors). These electrons are the principal cause of soft error in the memory LSI by alpha rays. That is, these electrons produce a noise current and, when a large noise current is produced, the stored information is destroyed. As an example, suppose that the n^+ BL **30** in which the electrons collect is the collector of the off-side transistor of FIG. **1A**, the electrons enter the collector of the off-side transistor, namely, the base of the on-side transistor **18**, as illustrated in FIG. **1A**. Thereby, the base voltage of the transistor **18** drops and the on-side transistor tends to become an off-state. When the charge of the electrons is large, the base voltage of the transistor **18** drops below the base voltage of the transistor **19**, and thereby the stored information is inverted.

Means previously taken prevent such soft error include: (1) preventing the incidence of alpha rays, (2) suppressing the accumulation of charge when the incidence of alpha rays occurs, or (3) providing the memory cell with noise current resistant characteristics. The first means is a well-known means in which the surface of the chip is coated with a film of a substance not containing any source of alpha rays having a thickness not less than several tens of microns. According to this means, the film having a thickness greater than the range of alpha rays, namely, the possible distance of intrusion of alpha rays into a substance, prevents alpha rays from reaching the silicon substrate. As the second means, appropriately controlling the distribution of the impurity concentration in the silicon substrate has been proposed. As the third means, inserting a capacitor between the collector node and the ground or a node equivalent to the ground from the viewpoint of AC has been proposed.

FIGS. **4A** to **4C** show examples of such means to prevent alpha rays. In the example shown in FIG. **4A**, capacitors are inserted between the collectors and the grounds, respectively, of the memory cell. The insertion of the capacitors suppresses the variation of the potential of the collectors even if a noise current is produced, and hence the possibility of soft error is reduced. The insertion of the capacitors as illustrated in FIG. **4A** enhances the immunity to soft error attributable to alpha rays, however, the time constant of the collector becomes large, which affects adversely to the high-speed performance of the bipolar memory. When capacitors are inserted as illustrated in FIG. **4B**, the capacitors function as a speed-up capacitor when the memory cell is driven, and hence this insertion of the capacitors improves both the operating speed and the immunity from alpha rays. However, those capacitors need to have a relatively large capacitance (not less than several fractions of a picofarad), and hence it is difficult to